FAIRCHILD
A Schlumberger Company

F6845/F6845A
CRT Controller

Microprocessor Product

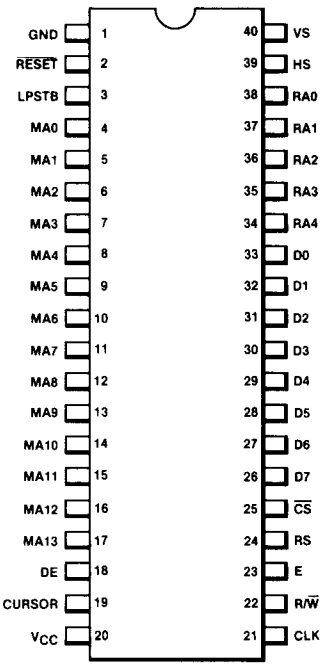
Description

The Fairchild F6845 CRT Controller (CRTC) provides an interface between a microprocessor (MPU) and a raster scan CRT device. The CRTC is used in microprocessor-based controller systems for CRT terminals in stand-alone or multiterminal configurations, including smart, programmable CRT terminals, video games, and information displays.

The F6845 CRTC is designed with an optimum hardware/software balance that achieves integration of all key functions and maintains flexibility. All keyboard functions, read/write operations, cursor movements, and editing are under microprocessor control. The F6845 provides video timing and refresh memory addressing.

- **Monochrome or Color CRT Applications**
- **Used with "Glass-Teletype", Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays**
- **Alphanumeric, Semigraphic, and Full Graphic Capability**
- **Fully Programmable via Processor Data Bus; Timing can be Generated for Almost Any Alphanumeric Screen Format (e.g., 80 x 24, 72 x 64, and 132 x 20)**
- **Single +5 V Supply**
- **F6800-Compatible Bus Interface**
- **TTL-Compatible Inputs and Outputs**
- **Start Address Register Provides Hardware Scroll (By Page, Line, or Character)**
- **Programmable Cursor Register Allows Control of Cursor Format and Blink Rate**
- **Light Pen Register**
- **Refresh (Screen) Memory Can Be Multiplexed Between the CRTC and the MPU, Thus Removing the Requirements for Line Buffers or External DMA Devices**
- **Programmable Interlace or Non-Interlace Scan Modes**
- **14-Bit Refresh Address Allows up to 16K of Refresh Memory for Use in Character or Semigraphic Displays**
- **5-Bit Row Address Allows up to 32 Scan-Line Character Blocks**
- **512K Address Space is Available for Graphics System by Using Both the Refresh and Row Addresses**
- **Refresh Addresses are Provided During Retrace, Allowing the CRTC to Provide Row Addresses to Refresh Dynamic RAM**
- **Programmable Skew for Cursor and Display Enable (DE)**

Connection Diagram



Signal Functions

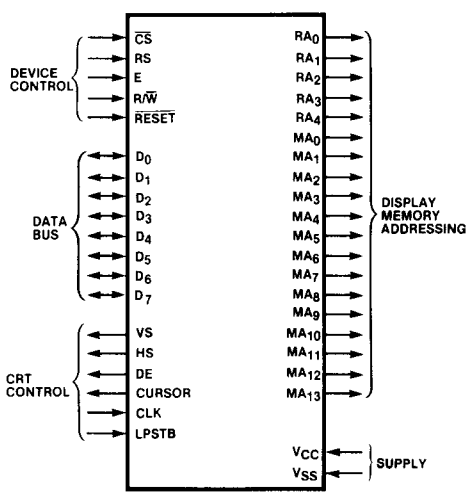


Figure 1 Non-Interlace Raster Scan System

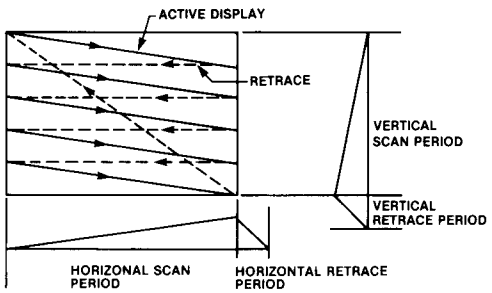
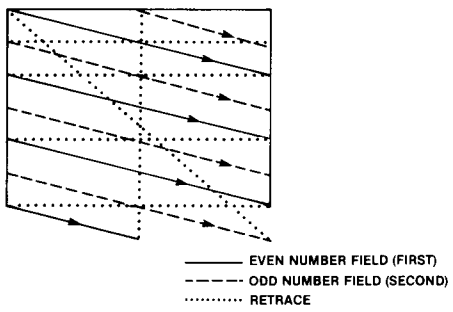


Figure 2 Interlace Raster Scan System



CRTC System Interface

The CRTC generates the signals necessary to interface a digital system to a raster scan CRT display. In this type of display, an electron beam starts in the upper left-hand corner, moves quickly across the screen, and returns. This action is called a horizontal scan. After each horizontal scan, the beam is incrementally moved down in the vertical direction until it has reached the bottom of the screen. At this point, one frame has been displayed, as the beam has made many horizontal scans and one vertical scan.

Two types of raster scanning are used in CRTs: interlace and non-interlace (illustrated in figures 1 and 2). Non-interlace scanning consists of one field per frame. The scan lines in figure 1 are shown as solid lines, and the retrace patterns are indicated by the dotted lines. Increasing the number of frames per second decreases the flicker. Ordinarily, either a 50 or 60 frame-per-second refresh rate is used to minimize beating between the CRT and the power line frequency. This prevents the displayed data from weaving.

Interlace scanning is used in broadcast TV and on data monitors where high-density or high-resolution data must be displayed. Two fields, or vertical scans, are made down the screen for each single picture or frame. The first field (even field) starts in the upper left-hand corner; the second (odd field) in the upper center. Both fields overlap as shown in figure 2, thus interlacing the two fields into a single frame.

To display the characters on the CRT screen, the frames must be continually repeated. The data to be displayed is stored in the refresh (screen) memory by the MPU controlling the data processing system. The data is usually written in ASCII code and cannot be directly displayed as characters. A character generator ROM is typically used to convert the ASCII codes into the "dot" pattern for every character.

The most common method of generating characters is to create a matrix of dots, x dots (columns) wide and y dots (rows) high. Each character is created by selectively filling in the dots. As x and y get larger, a more detailed character can be created. Two common dot matrices are 5 x 7 and 7 x 9. Many variations of these standards allow Chinese, Japanese, or Arabic letters instead of English. Since characters require some space between them, a character block larger than the character is typically used, as shown in figure 3. The figure also shows the corresponding timing and levels for a video signal that would generate the characters.

The CRTC generates the refresh addresses ($MA_0 - MA_{13}$), row addresses ($RA_0 - RA_4$), and the video timing — vertical synchronization (VS), horizontal synchronization (HS), and display enable (DE), as illustrated in figure 4. Other functions include an internal cursor register that generates a cursor output when its contents compare to the current refresh address. A light pen strobe input signal allows capture of the refresh address in an internal light pen register.

All timing in the CRTC is derived from the clock (CLK) input. In alphanumeric terminals, this signal is the character rate. The video rate, or dot clock, is externally divided by high-speed logic (TTL) to generate the CLK input. The high-speed logic also generates the timing and control signals necessary for the shift register, latch, and multiplexer control.

Figure 3 Character Display on the Screen and Video Signal

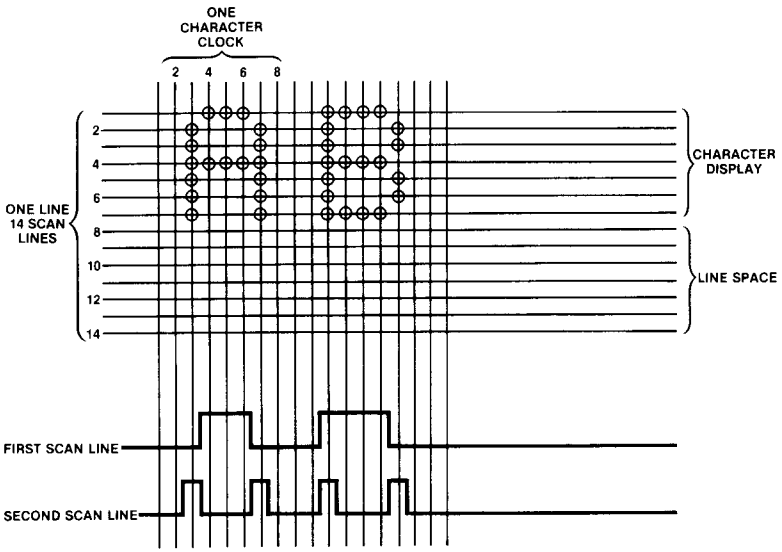
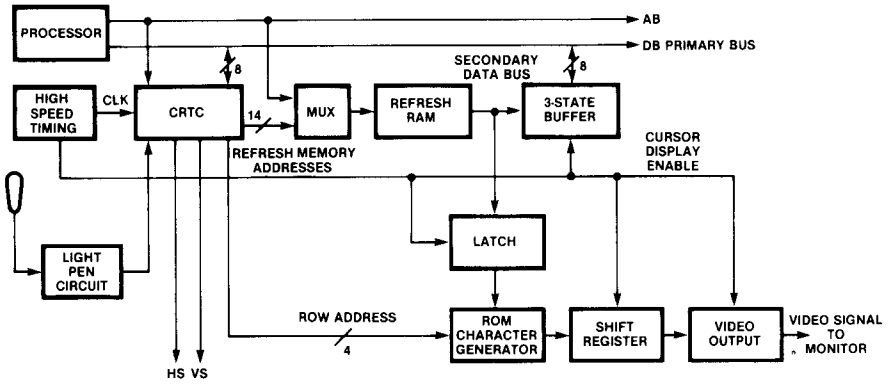


Figure 4 Typical CRT Controller Application



The processor communicates with the CRTC through an 8-bit data bus by reading or writing into the 19 registers. The refresh memory address is multiplexed between the microprocessor and the CRTC. Data appears on a secondary bus separate from the processor's primary bus. The secondary data bus concept in no way precludes using the refresh RAM for other purposes. It looks like any other RAM to the processor.

Refresh Memory Contentions

A number of approaches are possible for solving contentions in the refresh memory.

1. The processor always has priority. Generally, "hash" occurs, as the MPU and CRTC clocks are not synchronized.
2. The processor has priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.
3. The processor is synchronized with the memory wait cycles (states).
4. The processor is synchronized to the character rate as shown in figure 5. The F6800 processor family works very well in this configuration, as constant cycle lengths are present. This method provides no overhead for the processor, as there is never a contention for a memory access. All accesses are transparent.

The CRTC is offered in two pin-compatible versions. This data sheet contains information describing both the F6845 CRTC and the F6845A (upgraded) CRTC. Complete software compatibility between both versions is maintained by programming all register bits in the F6845A, which are undefined/unused in the F6845, with zeros.

The F6845 CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus. Figure 6 is a functional block diagram of the CRTC.

All CRTC timing is derived from the clock (CLK) input, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare the contents of the horizontal, horizontal sync width, character row, and scan line counters to the contents of the programmable register file, R_0 - R_{17}. For horizontal timing generation, comparisons result in the horizontal sync pulse (HS) of a frequency, position, and width determined by the registers, and the horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock, which drives the scan line counter and vertical control. The contents of the scan line register raster counter are continuously compared to the contents of the scan line address register. A coincidence resets the raster scan line counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in a vertical sync (VS) pulse of a frequency, width, and position determined by the registers, and a vertical display of a frequency and position determined by the registers. The width of the VSYNC pulse is fixed at 16 raster lines in the F6845. The vertical control logic has other functions, including the following.

1. Generates row selects or raster address RA_0 - RA_4 output from the raster count scan line for the corresponding interlace or non-interlace modes.
2. Extends the number of scan lines in the vertical total by the amount programmed in the vertical total adjust register.

The linear address generator is driven by CLK and associates the relative positions of characters in memory with their positions on the CRT screen. Fourteen refresh memory address lines, $MA_0 - MA_{13}$, are available for addressing up to four pages of 4K characters, eight pages of 2 K characters, etc. Using the start address register, hardware scrolling up to 16K characters is possible. The linear address generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blink rate on the CRT screen. All are programmable.

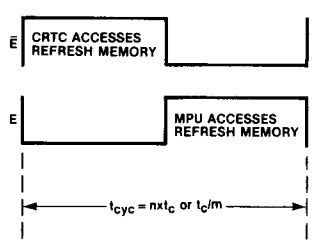
The light pen strobe (LPSTB) going high causes the current contents of the address counter to be latched in the light pen register. The contents of the light pen register are subsequently read by the microprocessor.

Internal CRTC registers are programmed by the microprocessor through the data bus, $D_0 - D_7$, and the control signals R/$\overline{W}$, $\overline{CS}$, RS, and E.

Signal Descriptions

The F6845 input/output signals are described in table 1.

Figure 5 Transparent Memory Configuration Timing Using F6800 MPU



Where m, n are integers and t_c is character period.

Figure 6 F6845 CRTC Block Diagram

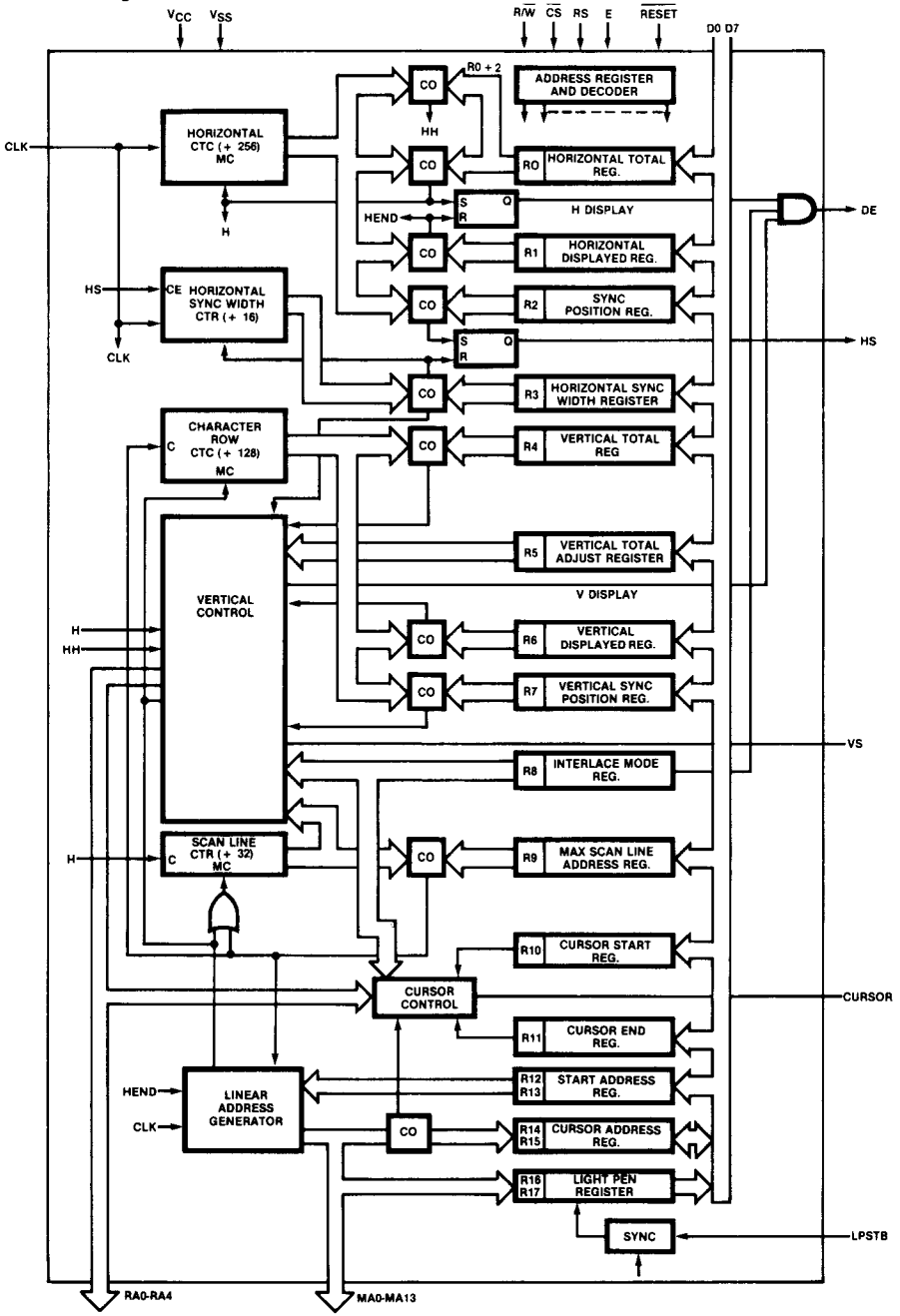


Table 1 F6845 CRTC Signal Descriptions

Mnemonic	Pin No.	Name	Description
Device Control			
$\overline{CS}$	25	Chip Select	High-impedance, TTL/MOS compatible input signal. When low, it selects the CRTC to allow reading from or writing to the internal register file. This signal should be active only when a valid stable address from the microprocessor is being decoded.
RS	24	Register Select	High-impedance, TTL/MOS compatible input signal. When low, it selects the address register; when high, it selects one of the data registers of the internal register file.
E	23	Enable	High-impedance, TTL/MOS compatible input signal. Enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the microprocessor clock; the high-to-low transition is the active edge.
R/$\overline{W}$	22	Read/Write	High-impedance, TTL/MOS compatible input signal. Determines whether the internal register file is written to or read from. A write operation is an active low (logic 0).
$\overline{RESET}$	2	Reset	An input signal used to reset the CRTC. When low, it clears all CRTC counters, stops display operations, and forces all outputs low; control registers in the CRTC are not affected and remain unchanged. The $\overline{RESET}$ signal performs a reset function only when the $\overline{LPSTB}$ signal is also low, as shown in the following. $\overline{RESET}$ — $\overline{LPSTB}$ — Operating Mode 0 — 0 — Reset 0 — 1 — Test 1 — 0 — Normal 1 — 1 — Normal The test mode configures the memory addresses as two independent 7-bit counters to minimize test time. After $\overline{RESET}$ goes low, the $MA_0 - MA_{13}$ and $RA_0 - RA_4$ signals, in synchronization with the CLK low level, also go low (at least one CLK signal is necessary for reset). The CRTC starts the display operation immediately after the release of the $\overline{RESET}$ signal. The DE signal is not active until after the first VS signal pulse occurs.

Mnemonic	Pin No.	Name	Description
Data Bus			
$D_0 - D_7$	26-33	Data Bus	Eight bidirectional data lines that allow data transfers between the CRTC internal register file and the microprocessor. The data bus output drivers are 3-state buffers that remain in the high-impedance state except when the microprocessor performs a CRTC read operation.
CRT Control			
VS	40	Vertical Synchronization	Active-high, TTL compatible output signal that determines the vertical position of the displayed text, drives the monitor directly, or is fed to video processing logic for composite generation.
HS	39	Horizontal Synchronization	Active-high, TTL compatible output signal that determines the horizontal position of the displayed text, drives the monitor directly or is fed to video processing logic for composite generation.
DE	18	Display Enable	Active-high, TTL compatible output signal that indicates the CRTC is providing addressing in the active display area.
CURSOR	19	Cursor	Active-high, TTL compatible output signal that indicates valid cursor address to external video processing logic.
CLK	21	Clock	A TTL/MOS compatible input signal that is used to synchronize all CRT control signals, except for the processor interface. An external dot counter is used to derive this signal, which is usually the character rate in an alphanumeric CRT. The active transition is from high to low.
LPSTB	3	Light Pen Strobe	High-impedance, TTL/MOS compatible input signal that latches the current refresh addresses into the light pen register file. Latching occurs on the low-to-high edge, and is internally synchronized to the character clock.
Display Memory Addressing			
$MA_0 - MA_{13}$	4-17	Refresh Memory Addresses	Output signals that are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. Drives a standard TTL load and 30 pF.
$RA_0 - RA_4$	34-38	Row Addresses	Output signals from the internal row address counter that address the character ROM for the row of a character. These signals drive a standard TTL load and 30 pF.
Supply			
V_{CC}	20	Supply Voltage	+5 V supply.
V_{SS}	1	Ground	Supply and signal ground.

Register Files

The 19 registers of the F6845 CRTC can be accessed through the data bus. Only two memory locations are required, as one location is used as a pointer to address one of the remaining 18 registers. These 18 registers control horizontal timing, vertical timing, interlace operation, and row address operation, and define the cursor, cursor address, start address, and light pen register. The register addresses and sizes are shown in table 2.

Table 2 CRTC Internal Register Assignment

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes	V_A	V_A	V_A	V_A	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char.Row	No	Yes								
0	1	0	0	1	0	1	R5	Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char.Row	No	Yes								
0	1	0	0	1	1	1	R7	Sync Position	Char.Row	No	Yes								
0	1	0	1	0	0	0	R8	Interlace Mode & Skew	Note 1	No	Yes	C_A	C_A	D_A	D_A			I	I
0	1	0	1	0	0	1	R9	Max.Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P			(Note 2)		
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	—	Yes	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	Yes	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

Notes

1. The skew control and interlace are described in the Interlace Mode and Skew Register section.
2. Bit 5 of the cursor start raster register is used for blink period control, and bit 6 is used to select blink or nonblink.
3. Subscript A represents the F6845A CRTC.

Address Register
The address register is a 5-bit write-only register used as an indirect or pointer register. It contains the address of one of the other 18 registers. When both the RS and $\overline{CS}$ signals are low, the address register is selected. When $\overline{CS}$ is low and RS is high, the register pointed to by the address register is selected.

Timing Registers R0-R9
The visible display area of a typical CRT monitor is shown in figure 7. The point of reference for horizontal registers is given as the left-most displayed character position. Horizontal registers are programmed in character clock time units with respect to the reference, as shown in figure 8. Signal characteristics are given in the "Timing Characteristics" section. The point of reference for the vertical registers is the top character position displayed. Vertical registers are programmed in scan line times with respect to the reference, as shown in figure 9.

Figure 7 F6845 CRT Screen Format

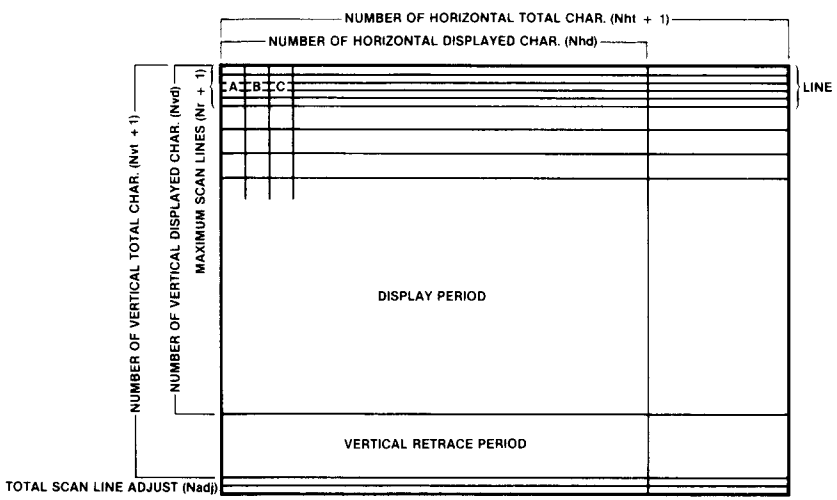
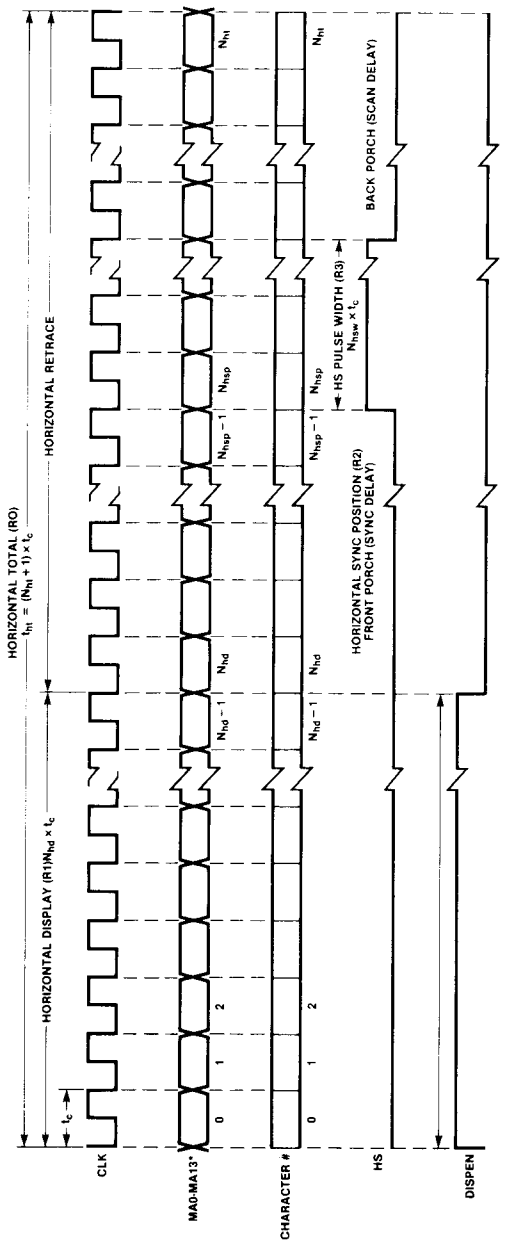
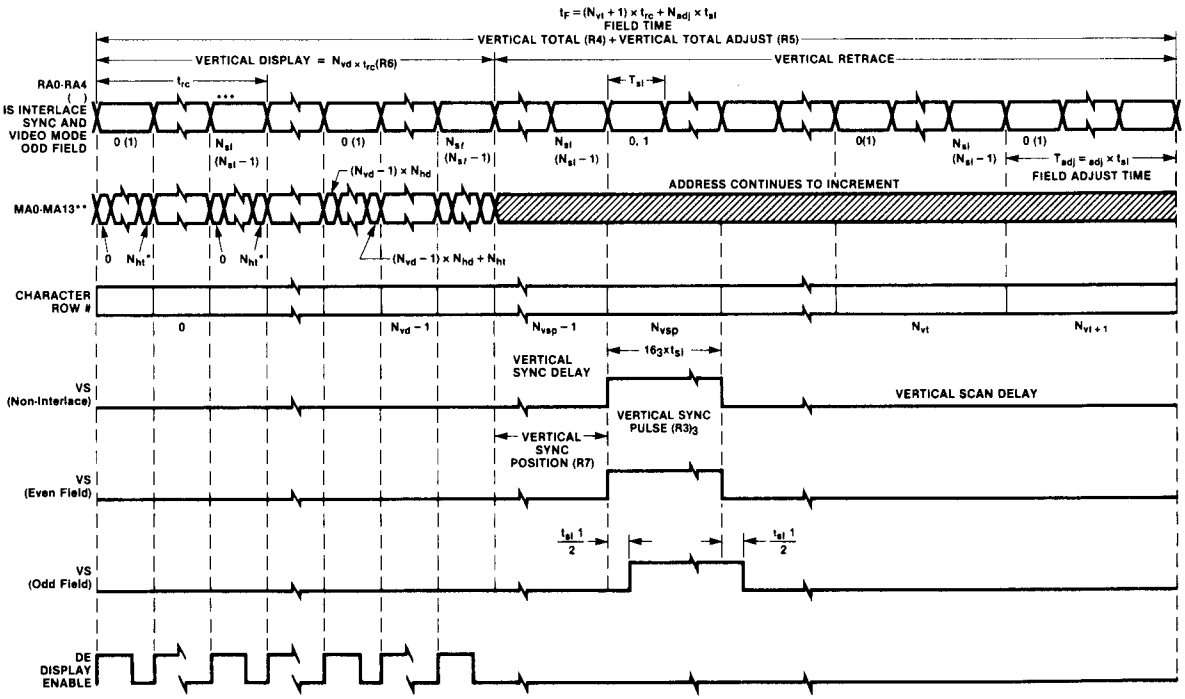


Figure 8 CRTC Horizontal Timing



Note
Timing is shown for first displayed scan row only. The initial MA is determined by the contents of start address register R_{12}/R_{13}. Timing is shown for $R_{12}/R_{13} = 0$.

Figure 9 CRTC Vertical Timing



*N_{ht} must be an odd number for both interlace modes.
**Initial MA is determined by R12/R13 (start address register), which is zero in this timing example.
***N_{sl} must be an odd number for interlace sync and video mode.

Notes:
1. Refer to Figure 2 - The odd field is offset ½ horizontal scan time.
2. Timing values are described in Table 9.
3. Vertical sync pulse width can be programmed from 1 to 16 scan line times for the MC6845 ☆ 1.

Horizontal Total Register (R0) - This 8-bit write-only register determines the horizontal sync (HSYNC) frequency by defining the period in character times. It is the total of the displayed characters plus the nondisplayed character times (retrace) minus one.

Horizontal Displayed Register (R1) - This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number can be programmed so long as the contents of R0 are greater than the contents of R1.

Horizontal Sync Position Register (R2) - This 8-bit write-only register controls the horizontal sync position, which defines the horizontal sync delay (Front Porch) and the horizontal scan delay (Back Porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased, the display is shifted to the right. Any 8-bit number can be programmed if the sum of the contents of R1, R2, and R3 is less than the contents of R0.

Sync Width Register (R3) - This 8-bit write-only register determines the width of the vertical sync pulse and the horizontal sync pulse for the F6845A CRTC. The vertical sync pulse width is fixed at 16 scan line times for the F6845, and the upper four bits of this register are treated as "don't cares".

The F6845A allows control of the VS pulse width for one to sixteen scan line times. Programming the upper four bits for one to fifteen selects pulse widths from one to fifteen scan line times. Programming the upper four bits as zeros selects a VS pulse width of 16 scan line times, allowing compatibility with the F6845.

For both the F6845 and the F6845A, the HS pulse width can be programmed from one to fifteen character clock periods, thus allowing compatibility with the HS pulse width specifications of many different monitors. If zero is written into this register, then no horizontal sync is provided.

This horizontal width must be programmed because, were it fixed as an integral of character times, it would vary with the character rate and be out of tolerance for certain monitors.

Horizontal Timing Summary - The difference between R0 and R1 is the horizontal blanking interval (refer to figure 8). This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor's horizontal scan components. Retrace time is less than the horizontal blanking interval.

A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers, the beam overscans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one-third the horizontal scanning period. The horizontal sync delay, HS pulse width, and horizontal scan delay are typically programmed with a 1:2:2 ratio.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) - The frequency of the VS pulse is determined by both the R4 and R5 registers. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed in the 5-bit write-only vertical total adjust register (R5) as a number of scan line times.

Vertical Displayed Register (R6) - This 7-bit write-only register specifies the number of displayed character rows on the CRT screen and is programmed in character row times. Any number smaller than the contents of the R4 register can be programmed into the R6 register.

Vertical Sync Position Register (R7) - This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. The value programmed in the register is one less than the number of computed character line times. When the programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number equal to or less than the vertical total (register R4) can be used.

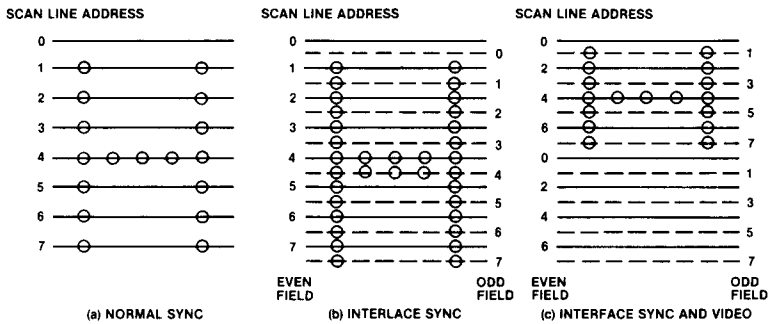
Table 3 Cursor and DE Skew Control

Value	Skew
00	No Character Skew
01	One Character Skew
10	Two Character Skew
11	Not Available

Table 4 Interlace Mode Register

Bit 1	Bit 0	Mode
0	0	Normal Sync Mode (Non-Interlace)
1	0	Normal Sync Mode (Non-Interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

Figure 10 Interlace Control



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Interlace Mode and Skew Register (R8) - The F6845 only allows control of the interlace modes as programmed by the low order two bits of this write-only register. The F6845A controls the interlace modes and allows a programmable delay of zero to two character clock times for the display enable (DE) and cursor outputs. Table 3 describes operation of the cursor and DE skew bits. Cursor skew is controlled by bits 6 and 7 of Register R8, while DE skew is controlled by bits 4 and 5. Table 4 shows the available interlace modes; these modes are selected using the two low order bits of this 6-bit write-only register. In the normal sync mode (non-interlace), only one field is available, as shown in figures 1 and 10 (a). Each scan line is refreshed at the VSYNC frequency (e.g., 50 or 60 Hz).

Two interlace modes are available, as shown in figures 2, 10 (b) and 10 (c). The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship VSYNC delayed by one-half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode, the same information is painted in both fields, as shown in figure 10 (b). This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, shown in figure 10 (c), alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given bandwidth of the CRT monitor.

To avoid an apparent flicker effect, care must be taken when using either interlace mode. This flicker effect is due to the doubling of the refresh time for all scan lines, since each field is displayed alaernately and can be minimized with proper monitor design (e.g., longer persistence phosphors).

In addition, the programming of the CRTC registers for interlace operation has the following restrictions.

F6845 Programming Restrictions

1. The horizontal total register value, R0, must be odd (i.e., an even number of character times).

2. For interlace sync and video mode only, the maximum scan line address, R9, must be odd (i.e., an even number of scan lines).

3. For interlace sync and video mode only, the vertical displayed register, R6, must be even. The programmed number, Nvd, must be one-half the actual number required. The even-numbered scan lines are displayed in the even field and the odd-numbered scan lines are displayed in the odd field.

4. For interlace sync and video mode only, the cursor start register, R10, and cursor end register, R11, must both be even or odd, depending in which field the cursor is to be displayed.

F6845A Programming Restrictions

1. The horizontal total register value, R0, must be odd (i.e., an even number of character times).

2. For the interlace sync and video mode only, the vertical displayed register, R6, must be even. The programmed number, Nvd, must be one-half the actual number required.

Maximum Scan Line Address Register (R9) - This 5-bit write-only register determines the number of scan lines per character row, including the spacing, thus controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

Figure 11 Cursor Control

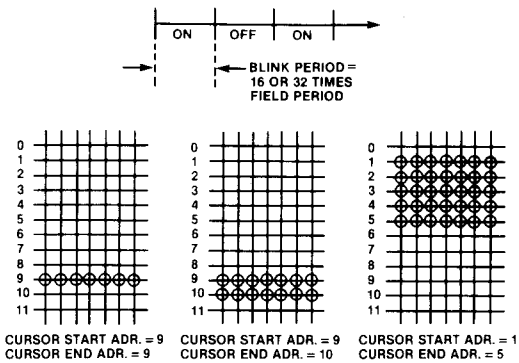


Table 5 Cursor Start Register

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Example of Cursor Display Mode

Cursor Control Registers-Cursor movement is controlled by the following four registers.

Cursor Start Register (R10) and Cursor End Register (R11) - These registers allow a cursor of up to 32 scan lines in height to be placed on any scan line of the character block, as shown in figure 11. Register R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the cursor start address register control the cursor operation, as shown in table 5. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. Register R11 is a 5-bit write-only register that defines the last scan line of the cursor.

Bit 5 is the blink timing control; when it is low, the blink frequency is 1/16 of the vertical field rate, and when it is high, the blink frequency is 1/32 of the vertical field rate. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower five bits.

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/noninvert cursor is easily implemented by programming the CRTC for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

Cursor Register (R14-H, R15-L) — This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area, thus allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low order ($MA_0 - MA_7$) register and a 6-bit high order ($MA_8 - MA_{13}$) register.

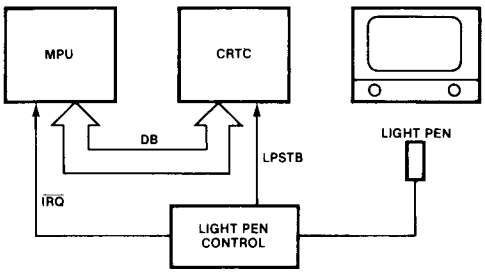
Start Address and Light Pen Registers

The following 14-bit registers control the start address and light pen.

Start Address Register (R12-H, R13-L) — This 14-bit write-only register pair controls the first address by the CRTC after vertical blanking. It consists of an 8-bit low order ($MA_0 - MA_7$) register and a 6-bit high order ($MA_8 - MA_{13}$) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Because the CRTC linear address generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16 block of refresh memory. Hardware scrolling by characters, line, or page can be accomplished by centering the R12/R13 pointer in the middle of the available memory space.

Light Pen Register (R16-H, R17-L) - This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low order (MA_0-MA_7) register and a 6-bit high order (MA_0-MA_{13}) register. Since the light pen pulse is aynchronous with respect to refresh address timing, an internal synchronizer is designed into the CRTC. Due to delays in this circuit, the value of R16 and R17 need to be corrected in software. (See the bus timing diagram in the Timing Characteristics section). Figure 12 shows an interrupt-driven approach, although a polling routine could be used.

Figure 12 Light Pen Interface



CRTC Initialization

Registers R0-R15 must be initialized after the system power is turned on. The processor normally loads the CRTC register file sequentially from a firmware table, after which, in most systems, R0-R11 are not changed. The worksheet of table 6 is useful in computing proper register values for the CRTC. Table 6 shows the worksheet completed for an 80 × 24 configuration using a 7 × 9 character generator, and figure 13 shows an F6800 program that could be used to program the CRT controller. The programmed values allow use of either an F6845 or an F6845A CRTC.

The CRTC registers have an initial value at power up. When using a direct drive monitor (without horizontal oscillator), these initial values can result in out-of-tolerance operation. The CTRC programming should be done immediately after power up, especially in this type of system.

CRT Interface Signal Timing

Timing charts of CRT interface signals are illustrated with the aid of a programmed example of the CRTC. When values listed in table 7 are programmed into the CRTC control registers, the device provides the outputs as shown in the timing diagrams (figure 8, 9, 14, and 15). The screen format of this example is shown in figure 7, which illustrates the relation between refresh memory address (MA_0-MA_{13}), row address (RA_0-RA_4), and the position on the screen. In this example, the start address is assumed to be zero.

The bus timing test load is shown in figure 16; figure 17 illustrates the CRTC timing, and figure 18 illustrates the CRTC clock, memory addressing, and light pen timing. All signal timing characteristics are given in the "Timing Characteristics" section of this data sheet.

Additional CRTC Applications

The foremost system function that can be performed by the CRTC is the refreshing of dynamic RAM. This is quite simple, as the refresh addresses run continually.

Note that the LPSTB input signal can be used to support additional system function other than a light pen. A digital-to-analog converter (DAC) and comparator could be configured to use the refresh addresses as a reference to a DAC composed of a resistive adder network connected to a comparator. The output of the comparator generates the LPSTB input signal, signifying a match between the refresh address analog level and the unknown voltage.

The light pen strobe input could also be used as a character strobe to allow the CRTC refresh addresses to decode a keyboard matrix. Debouncing would need to be done in software.

Both the VS and HS signal outputs can be used as a real-time clock. Once programmed, the CRTC provides a stable reference frequency.

Table 6 Worksheet for 80 x 24 Format

Display Format Worksheet		
1. Displayed Characters per Row	80	Char.
2. Displayed Character Rows per Screen	24	Rows
3. Character Matrix a. Columns	7	Columns
b. Rows	9	Rows
4. Character Block a. Columns	9	Columns
b. Rows	11	Rows
5. Frame Refresh Rate	60	H_z
6. Horizontal Oscillator Frequency	16,600	H_z
7. Active Scan Lines (Line 2 x Line 4b)	264	Lines
8. Total Scan Lines (Line 6 ÷ Line 5)	310	Lines
9. Total Rows Per Screen (Line 8 ÷ Line 4b)	28	Rows and 2 Lines
10. Vertical Sync Delay (Character Rows)		Rows
11. Vertical Sync Width (Scan Lines, 16)	16	Lines
12. Horizontal Sync Delay (Character Times)	6	Character Times
13. Horizontal Sync Width (Character Times)	9	Character Times
14. Horizontal Scan Delay (Character Times)	7	Character Times
15. Total Character Times (Lines 1 + 12 + 13 + 14)	102	Character Times
16. Character Rate (Line 6 times 15)	1.8972 M	MH_z
17. Dot Clock Rate (Line 4a times 16)	17.075 M	MH_z

CRTC Registers

		Decimal	Hex
R0	Horizontal Total (Line 15 minus 1)	101	65
R1	Horizontal Displayed (Line 1)	80	50
R2	Horizontal Sync Position (Line 1 + Line 12)	86	56
R3	Horizontal Sync Width (Line 13)	9	9
R4	Vertical Total (Line 9 minus 1)	24	18
R5	Vertical Adjust (Line 9 Lines)	10	0A
R6	Vertical Displayed (Line 2)	24	18
R7	Vertical Sync Position (Line 2 + Line 10)	24	18
R8	Interlace (00 Normal, 01 Interlace 03 Interlace, and Vidio)		0
R9	Max. Scan Line Add (Line 4b minus 1)	11	B
R10	Cursor Start	0	0
R11	Cursor End	11	B
R12, R13	Start Address (H and L)	128	00 80
R14, R15	Cursor (H and L)	128	00 80

Figure 13 F6800 Program for CRTC Initialization

Page 001 CRTC INIT. SA:0 F6845/F6845-1 CTRC initialization program

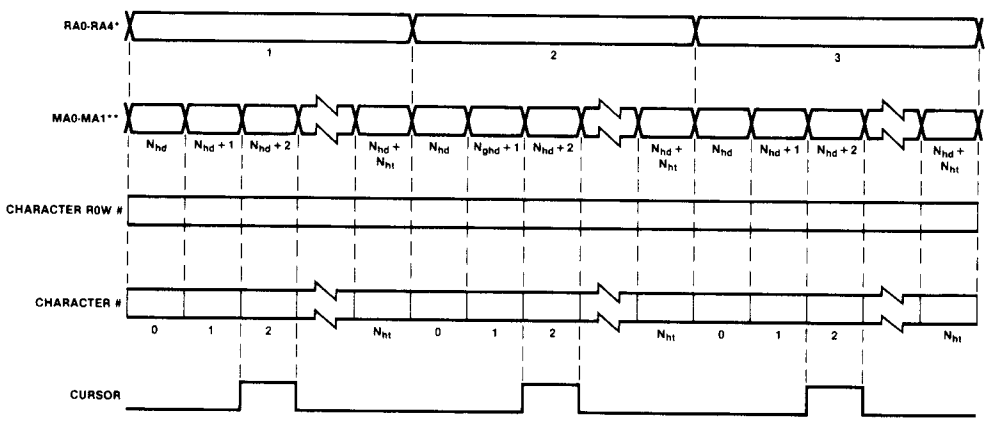
```
00001                          NAM   F6845
00002                          TTL   F6845-1      CRTC initialization program
00003                          OPT   G,S,LLE=85 print FCB's, FDB's & XREF table
00004                  ********************************************************
00005                  *Assign  CRTC  addresses
00006                  *
00007                  CRTCAD  EQU   $9000        Address Register
00008                  CRTCRG  EQU   CRTCAD+1     Data Register
00009                  ********************************************************
00010                  * Initialization program
00011                  *
00012A 0000                    ORG   0            a place to start
00013A 0000 5F                 CLRB               clear counter
00014A 0001 CE 1020 A          LDX   #CRTTAB      table pointer
00015A 0004 F7 9000 A  CRTC1   STAB  CRTCAD       load address register
00016A 0007 A6 00    A         LDAA  0,X          get register value from table
00017A 0009 B7 9001 A          STAA  CRTCRG       program register
00018A 000C 08                 INX                increment counters
00019A 000D 5C                 INCB
00020A 000E C1 10    A         CMPB  $10          finished?
00021A 0010 26 F2 0004         BNE   CRTC1        no: take branch
00022A 0012 3F                 SWI                yes: call monitor
00023                  ********************************************************
00024                  * CRTC register initialization table
00025                  *
00026A 1020                    ORG   $1020        start of table
00027A 1020    65    A  CRTTAB FCB   $65,$50      R0, R1 - total & H displayed
     A 1021    50    A
00028A 1022    56    A         FCB   $56,$09      R2, R3 - pos. & HS width
     A 1023    09    A
00029A 1024    18    A         FCB   $18,$0A      R4, R5 - V total & V total adj.
     A 1025    0A    A
00030A 1026    18    A         FCB   $18,$18      R6, R7 - V displayed & VS pos.
     A 1027    18    A
00031A 1028    00    A         FCB   $00,$0B      R8, R9 - Interlace & Max scan line
     A 1029    0B    A
00032A 102A    00    A         FCB   $00,$0B      R10,R11 - Cursor start & end
     A 102B    0B    A
00033A 102C    0080  A         FDB   $0080        R12,R13 - Start Address
00034A 102E    0080  A         FDB   $0080        R14,R15 - Cursor Address
00035                  END
Total Errors 00000--00000

CRTCL  0004  CRTCAD 9000  CRTCRG 9001  CRTTAB 1020
```

Table 7 Values Programmed Into CRTC Registers

Reg.#	Register Name	Value	Programmed Value
R0	Horizontal Total	$N_{ht} + 1$	N_{ht}
R1	Horizontal Displayed	N_{hd}	N_{hd}
R2	Horizontal Sync Position	N_{hsp}	N_{hsp}
R3	Horizontal Sync Width	N_{hsw}	N_{hsw}
R4	Vertical Total	$N_{vt} + 1$	N_{vt}
R5	Vertical Scan Line Adjust	N_{adj}	N_{adj}
R6	Vertical Displayed	N_{vd}	N_{vd}
R7	Vertical Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start	1	
R11	Cursor End	3	
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)	0	
R15	Cursor (L)	2	
R16	Light Pen (H)		
R17	Light Pen (L)		

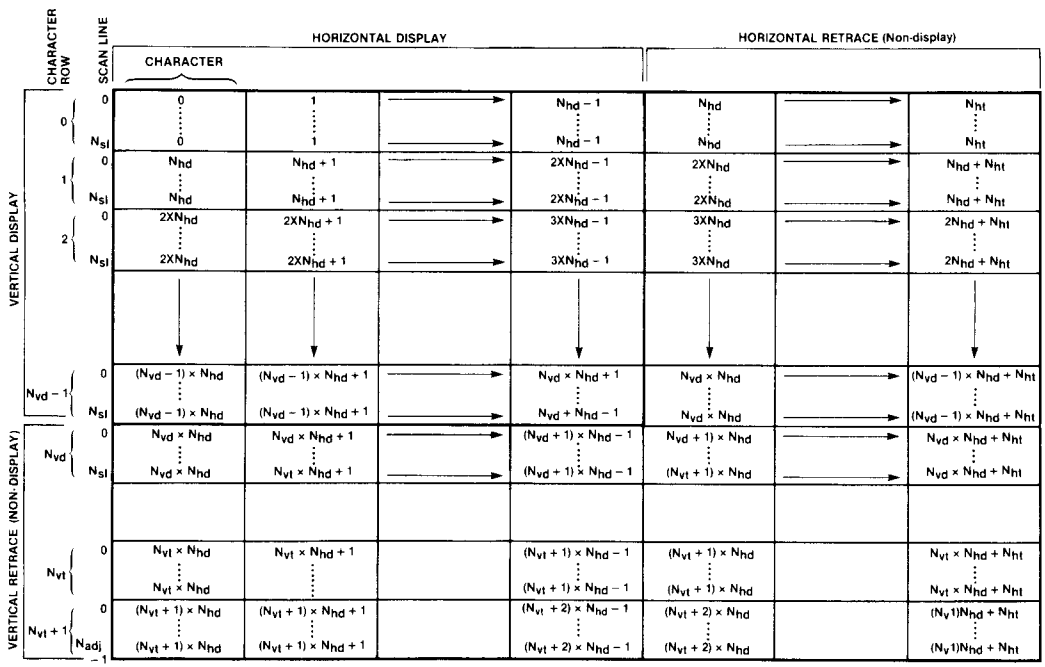
Figure 14 Cursor Timing Diagram



*Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as
Cursor Register = $N_{hd} + 2$
Cursor Start = 1
Cursor End = 3

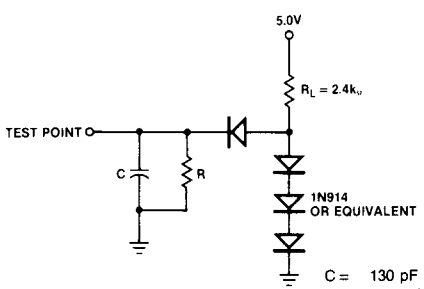
**The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/13 = 0

Figure 15 Refresh Memory Addressing ($MA_0 - MA_{13}$) Timing Diagram



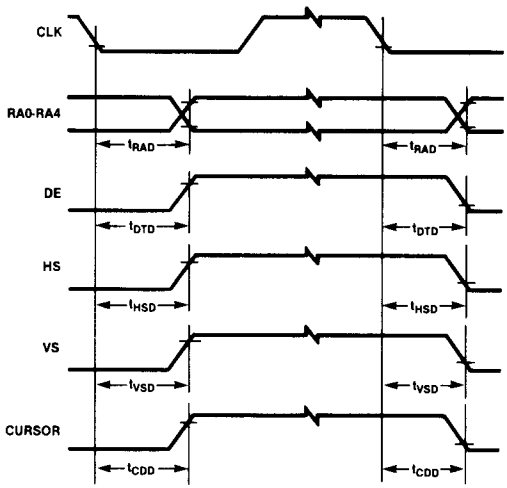
Note 1: The initial MA is determined by the contents of start register, R12/R13. Timing is shown for R12/R13=0. Only non-interlace and interlace sync modes are shown.

Figure 16 CRTC Bus Timing Test Load



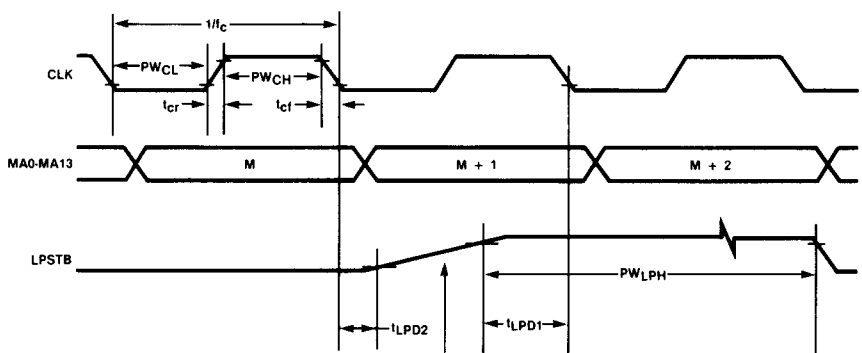
C = 130 pF for D0-D7
= 30 pF for MA0-MA13, RA0-RA4, DE, HS, VS, and CURSOR
R = 11 kΩ for D0-D7
= 24 for All Other Outputs

Figure 17 CRTC Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

Figure 18 CRTC Clock, Memory Addressing, and Light Pen Timing Diagram

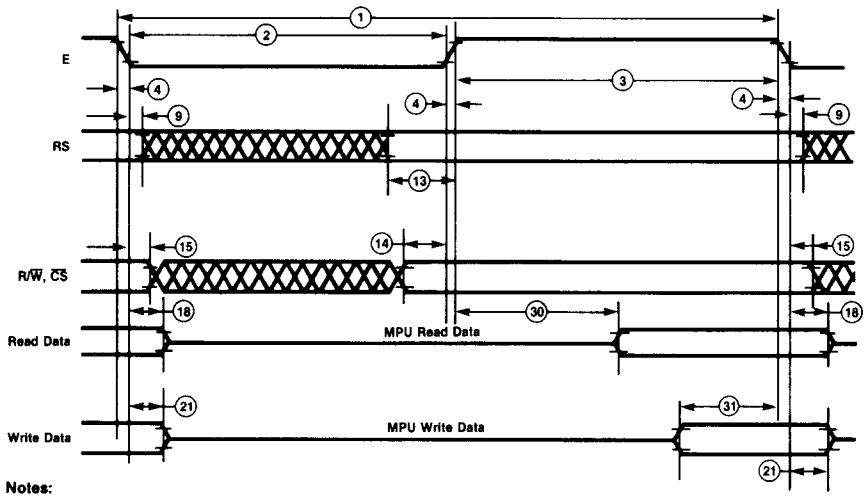


Note: Timing measurements are referenced to and from a low voltage of 0.8 volts, and a high voltage of 2.0 volts, unless otherwise noted.

Timing Characteristics

The signal timing for the CRTC bus is shown in figure *19*; ac characteristics for the bus timing are given in table *8*, and for the CRTC timing in table 9.

Figure 19 CRTC Bus Timing Diagram



Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

Table 8 CRTC Bus Timing Characteristics

Ident. Number	Characteristic	Symbol	F6845/ F6845A		F68A45/ F68A45A		F68B45/ F68B45A		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	20	500	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
9	Address Hold Time (RS)	t_{AH}	10	—	10	—	10	—	ns
13	RS Setup Time Before E	t_{AS}	80	—	60	—	40	—	ns
14	R/W and CS Setup Time Before E	t_{CS}	80	—	60	—	40	—	ns
15	R/W and CS Hold Time	t_{CH}	10	—	10	—	10	—	ns
18	Read Data Hold Time	t_{DHR}	20	50•	20	50•	20	50•	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	ns
30	Peripheral Output Data Delay Time	t_{DDR}	—	290	—	180	0	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	—	80	—	60	—	ns

• The data bus output buffers are no longer sourcing or sinking current by t_{DHR} max (high impedance).