Z765A FDC
Floppy Disk Controller

October 1988

FEATURES

Address Mark detection circuitry internal to the FDC simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable.

Z765A features are:

- IBM-compatible format, Single and Double Density
- Multisector and multitrack transfer capability
- Data scan capability—scans a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- Drives up to 4 floppy-disk drives (FDD)
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Compatible with most general-purpose microprocessors
- Single phase 8 MHz clock
- +5V Only
- **40-Pin Dual-In-Line (DIP) package, 44-Pin plastic chip carrier (PLCC) package.**

GENERAL DESCRIPTION

The Z765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to four floppy-disk drives. It supports IBM System 3740 Single Density format (FM) and IBM System 34 Double Density format (MFM) including double-sided recording. The Z765A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface. (Figure 1).

Handshaking signals make DMA operation easily incorporated with the aid of an external DMA Controller chip, such as the Z80 DMA. The FDC operates in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

The Z765A executes 15 commands; each command requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The commands are:

- READ DATA
- WRITE DATA
- WRITE DELETED DATA
- READ DELETED DATA
- READ TRACK
- READ ID
- FORMAT TRACK
- SCAN EQUAL
- SCAN HIGH OR EQUAL
- SCAN LOW OR EQUAL
- SEEK
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DRIVE STATUS

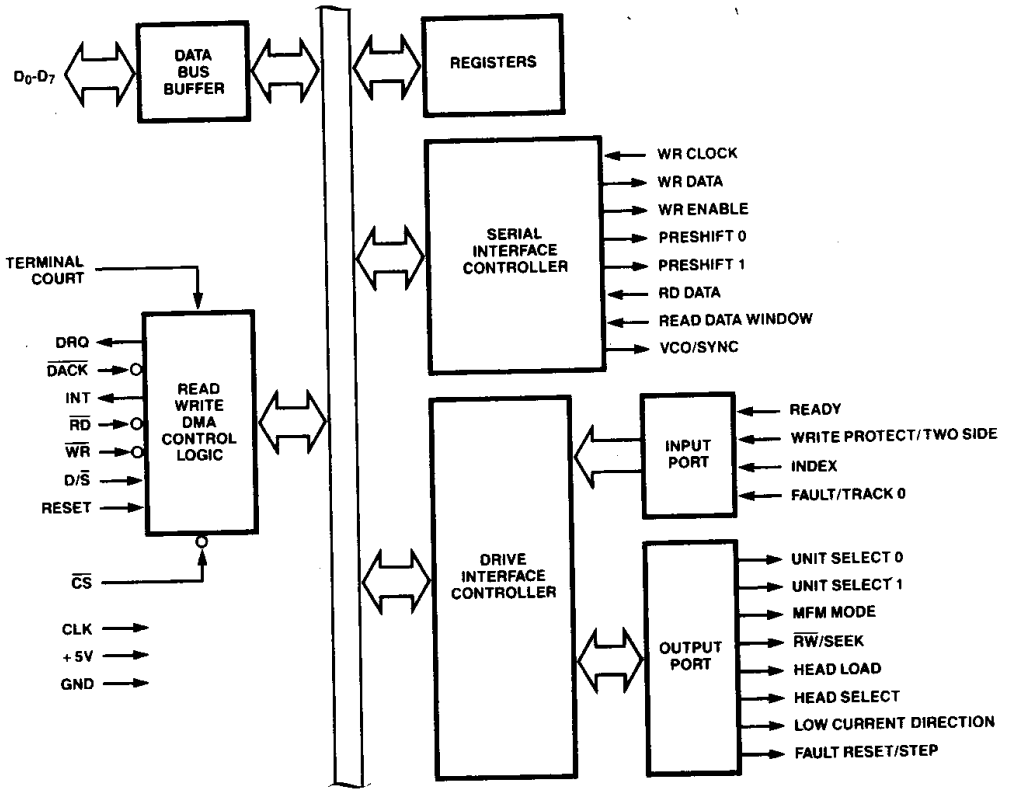

Figure 1. Z765A FDC Block Diagram

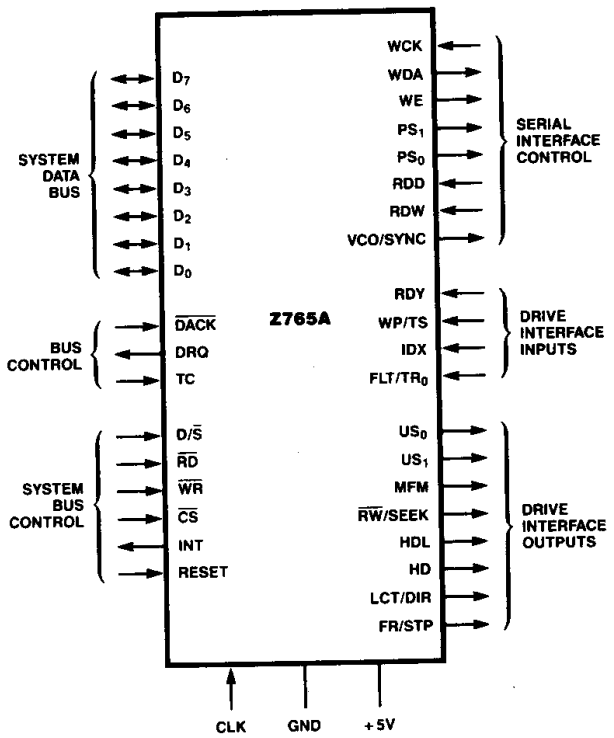

Figure 2. Pin Functions

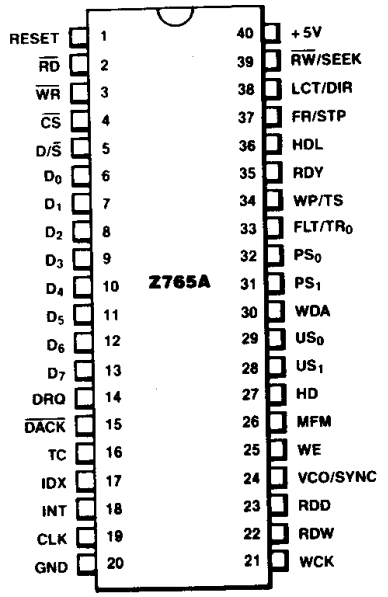

Figure 3a. Pin Assignments

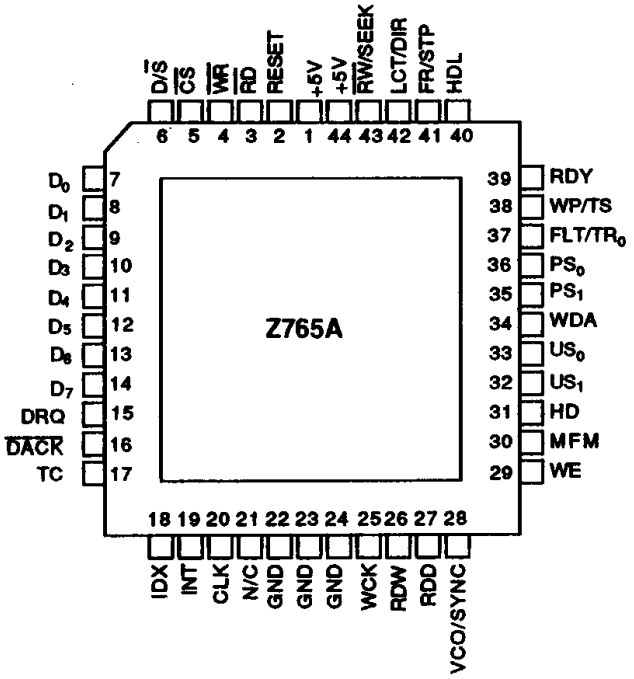

Figure 3b. Pin Assignments

PIN DESCRIPTIONS (Figures 2 and 3)

CLK. *Clock* (input). Single phase 8MHz square wave clock.

$\overline{CS}$. *Chip Select* (input). IC selected when 0 (Low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.

D_0-D_7. *Data Bus.* Bidirectional 8-bit Data Bus. Disabled when $\overline{CS}$ = 1.

$\overline{DACK}$. *DMA Acknowledge* (input). DMA cycle is active when 0, and controller is performing DMA transfer.

DRQ. *Data DMA Request* (output). DMA Request is being made by FDC when DRQ = 1.

D/$\overline{S}$. *Data/Status Register Select* (input). Selects Data Register (D/$\overline{S}$ = 1) or Status Register (D/$\overline{S}$ = 0) contents of the FDC to be sent to Data Bus. Disabled when $\overline{CS}$ = 1.

FR/STP. *Fault Reset/Step* (output). Resets fault FF in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.

FLT/TR_0. *Fault/Track 0* (input). Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.

HD. *Head Select* (output). Head 1 selected when 1 (High); Head 0 selected when 0 (Low).

HDL. *Head Load* (output). Command which causes read/write head in FDD to contact diskette.

IDX. *Index* (input). Indicates the beginning of a disk track.

INT. *Interrupt* (output). Interrupt Request generated by FDC.

LCT/DIR. *Low Current/Direction* (output). Lowers Write current on inner tracks in Read/Write mode; determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.

MFM. *MFM Mode* (output). MFM mode when 1; FM mode when 0.

PS_1, PS_0. *Precompensation (preshift)* (output). Write precompensation status during MFM mode. Determines early, late, and normal times.

$\overline{RD}$. *Read* (input). When 0, control signal for transfer of data from FDC to Data Bus. Disabled when $\overline{CS}$ = 1.

RDD. *Read Data* (input). Read data from FDD, containing clock and data bits.

RDW. *Read Data Window* (input). Generated by PLL, and used to sample data from FDD.

RDY. *Ready* (input). Indicates FDD is ready to send or receive data.

RESET. *Reset* (input). Places FDC in idle state. Resets output lines to FDD to 0. Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held High during Reset, FDC generates an interrupt within 1.024 msec. To clear this interrupt use Sense Interrupt Status command.

$\overline{RW}$/SEEK. *Read Write/Seek* (output). When 1 (High) Seek mode selected; when 0 (Low) Read/Write mode selected.

TC. *Terminal Count* (input). Indicates the termination of a DMA transfer when 1 (High). It terminates data transfer during Read/Write/Scan command in DMA or Interrupt mode.

US_1, US_0. *Unit Select* (output). FDD Unit selected.

VCO/SYNC. (output). Inhibits VCO in PLL when 0 (Low); enables VCO when 1.

WCK. *Write Clock* (input). Write data rate to FDD. FM = 500 KHz, MFM = 1 MHz with a pulse width of 250 ns for both FM and MFM.

WDA. *Write Data* (output). Serial clock and data bits to FDD.

WE. *Write Enable* (output). Enables write data into FDD.

WP/TS. *Write Protect/Two Side* (input). Senses Write Protect status in Read/Write mode and Two-Side Media in Seek mode.

$\overline{WR}$. *Write* (input). When 0, control signal for transfer of data to FDC via Data Bus. Disabled when $\overline{CS}$ = 1.

Table 1. Internal Registers

The bits in the Main Status Register are defined as follows:

Bit No.	Name	Symbol	Description
D_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
D_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When D_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
D_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, transfer is from the processor to Data Register.
D_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

INTERNAL REGISTERS

The Z765A contains two registers which may be accessed by the main system processor: a Status register and a Data register. The 8-bit Main Status register (Table 1) contains the FDC status information and may be accessed at any time. The 8-bit Data register is several registers in a stack; one register at a time is presented to the data bus. The Data register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data register in order to program or obtain the results after a particular command. Only the Status register may be read and used to facilitate the transfer of data between the processor and Z765A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and $D/\overline{S}$ is shown in Table 2.

The Data Input/Output (DIO) and Request for Master (RQM) bits in the Status register indicate when data is ready and the direction transfer on the data bus (Figure 4). The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and the set or reset DIO and RQM is 12μs; every time the Main Status register is read the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when D_4 (FDC busy) goes Low is 12μs.

Table 2. Relationships Between Status/Data Registers and $\overline{RD}$, $\overline{WR}$, and $D/\overline{S}$

$D/\overline{S}$	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

STATUS REGISTER IDENTIFICATION

Bit No.	Name	Symbol	Description
			Status Register 0
D_7 D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed.
			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK command, this flag is set to 1 (High).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US_1	This flag is used to indicate a Drive Unit Number at Interrupt.
D_0	Unit Select 0	US_0	This flag is used to indicate a Drive Unit Number at Interrupt.
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (Low).
D_5	Data Error	DE	When the FDC detects a Cyclic Redundancy Check (CRC) error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (Low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN command, if the FDC cannot find the sector specified in the Internal Data Register (IDR), this flag is set.
			During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the READ A cylinder command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (Continued)

Bit No.	Name	Symbol	Description
			Status Register 1 (Continued)
D_1	Not Writeable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in data field) of Status register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (Low).
D_6	Control Mark	CM	During execution of the READ DATA or SCAN command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of Cylinder (C) on the medium is different from that stored in IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF_H, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			Status Register 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the FDD.
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the Unt Select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

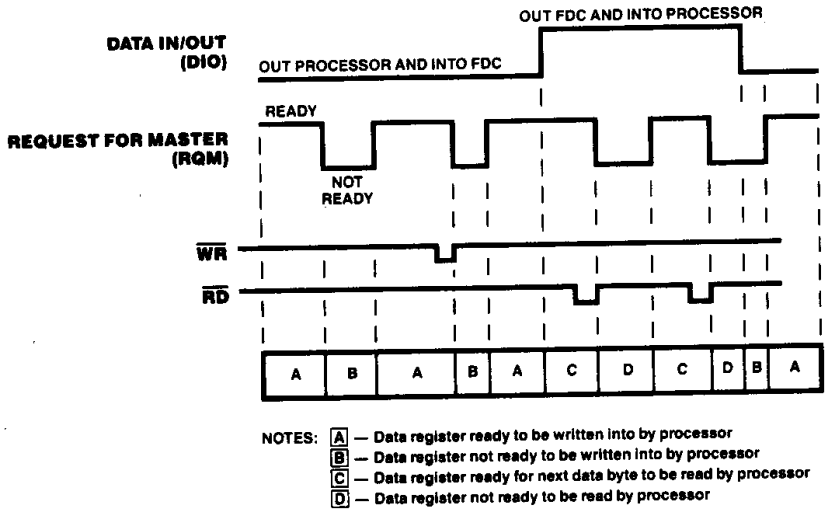

Figure 4. Data Transfer

COMMAND SEQUENCE

The Z765A is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor; the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the Z765A and the processor, each command consists of three phases:

Command Phase. The FDC receives all information required to perform a particular operation form the processor.

Execution Phase. The FDC performs the operation it was instructed to do.

Result Phase. After completion of the operation, status and other housekeeping information are made available to the processor.

The Instruction set shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The W to the left of each byte indicates a command phase byte to be written; an R indicates a result byte.

PROCESSOR INTERFACE

During Command or Result phases the Main Status register must be read by the processor before each byte of information is written into, or read from, the Data register. Then the CPU should wait for 12μs before reading the Main Status register. Bits D_6 and D_7 in the Main Status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the Z765A. Many of the commands require multiple bytes and, as a result, the Main Status register must be read prior to each byte transfer to the Z765A. During the Result phase, D_6 and D_7 in the Main Status register must both be 1's before reading each byte from the Data Register. Reading the Main Status register before each byte transfer to the Z765A is required only in the Command and Result phases, not during the Execution phase.

If the Z765A is in the non-DMA mode and reading data from FDD, then the receipt of each data byte is indicated by an interrupt signal on pin 18(INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will clear the interrupt and output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status register and bit D_7 (RQM) functions as the interrupt signal. If a Write command is in process, the $\overline{WR}$ signal negates the reset to the interrupt signal.

In the non-DMA mode it is necessary to examine the Main Status register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the Z765A is in the

COMMAND SYMBOL DESCRIPTION

Symbol	Name	Description
D/$\overline{S}$	Data/Status Select	D/$\overline{S}$ controls selection of Main Status register (D/$\overline{S}$ = 0) or Data register (D/$\overline{S}$ = 1)
C	Cylinder Number	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCO/SYNC will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is Low, FM mode is selected, and if it is High. MFM mode is selected.
MT	Multitrack	If MT is high, a Multitrack operation is performed. If MT = 1 after finishing Read/Write operation on side 0, FDC automatically starts searching for sector 1 on side 1.
N	Number	N stands for the Number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a New Cylinder Number or desired position of head which is going to be reached as a result of the Seek operation.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number or present position of Head at the completion of Sense Interrupt Status command.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives ($F_{(16)}$ = 1 ms, $E_{(16)}$ = 2 ms, $D_{(16)}$ = 3 ms, . . .).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by D/$\overline{S}$ = 0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	Step	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US_0, US_1	Unit Select	Used to select between drives 0-3.

INSTRUCTION SET[1, 2]

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					Read Data					
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	See Note 3
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
					Read Deleted Data					
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					Write Data					
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector IC information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								
					Write Deleted Data					
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

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INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					Read A Track					
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
					Read ID					
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information read during Execution phase from Floppy Disk.
	R	H								
	R	R								
	R	N								

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3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					Format A Track					
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	N								Bytes Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler byte
Execution										FDC formats an entire track.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								In this case, the ID information has no meaning.
	R	H								
	R	R								
	R	N								
					Scan Equal					
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data compared between the FDD and the main system.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to Track 0

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information about the FDC at the end of seek operation
	R	PCN								
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT							HUT	
	W	HLT							ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	ST3								Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	Invalid Codes								Invalid Command Codes (NoOp—FDC goes into Standby state.)
Result	R	ST0								ST0 = $80_{(H)}$

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

DMA mode, no interrupts are generated during the Execution phase. The Z765A generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ (DMA Acknowledge) = 0 and an $\overline{RD}$ (Read signal) = 0. When the DMA Acknowledge signal goes Low ($\overline{DACK}$ = 0), then the DMA request is cleared (DRQ = 0). If a Write command has been issued, a $\overline{WR}$ signal appears instead of $\overline{RD}$. After the Execution phase has been completed [Terminal Count (TC) has occurred] or the last sector on the cylinder (EOT) read/written, then an interrupt occurs (INT = 1) which signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

During the Result phase all bytes shown in the Command Table must be read. For example, the Read Data command has seven bytes of data in the Result phase; all seven bytes must be read to successfully complete the Read Data command and allow the Z765A to accept a new command.

The Z765A contains five Status registers. The Main Status register can be read at any time by the processor. The other four Status registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and can be read only after completing a command. The particular command that has been executed determines how many of the Status registers are read.

The bytes of data which are sent to the Z765A to form the Command phase and are read out of the Z765A in the Result phase must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the Z765A, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the Z765A is ready for a new command.

POLLING FEATURE OF THE Z765A

After Reset is sent to the Z765A, the Unit Select lines US_0 and US_1 automatically go into a polling mode (Figure 5). Between commands (and between step pulses in the Seek command) the Z765A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing), then the Z765A generates an interrupt. When Status register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) is indicated. The polling of the Ready line by the Z765A occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms.

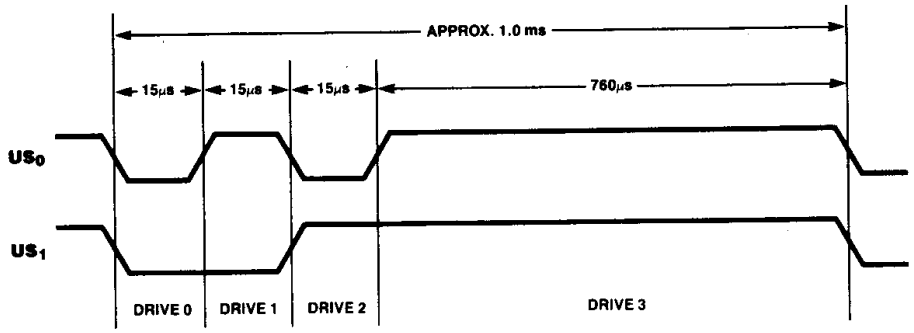


Figure 5. Polling Features

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command is issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC, via the data bus, outputs data byte-to-byte from the data field to the main system.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a Multi-Sector Read Operation. The Read Data command can be terminated by the receipt of a TC signal which should be issued when the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but continues to read data from the current sector, checks Cyclic Redundancy Count (CRC), and at the end of the sector, terminates the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon multitrack (MT), MFM/FM (MF), and Number of Bytes/Sector (N). Table 3 shows the Transfer Capacity.

Table 3. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

MT allows the FDC to read data from both sides of the diskette. For a particular cylinder, data is transferred starting at Sector 1, Side 0 and completing at the last sector, Sector L, Side 1. This function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC internally reads the complete sector performing the CRC check and, depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF_H.

At the completion of the Read Data Command the head is unloaded, after the Head Unload Time Interval specified in the Specify Command has elapsed. If the processor issues another command before the head unloads, there is no head settling time between subsequent reads. This time saved is particularly valuable when a diskette is copied.

If the FDC twice detects the index hole without finding the right sector (R), then the FDC sets Status register 1's No Data (ND) flag to 1, and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data fields in each sector, the FDC checks the CRC bytes. If a read error is detected indicating incorrect CRC in the ID field, the FDC sets Status register 1's Data Error (DE) flag to 1, and if a CRC error occurs in the Data Field, the FDC also sets Status register 2's Data Error in Data Field (DD) flag to 1, and terminates the Read Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit D in the first Command Word = 0, then the FDC sets Status register 2's Control Mark (CM) flag to 1, and after reading all the data in the sector, terminates the Read Data command. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. When SK = 1, the CRC bits in the deleted data field are not checked.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27μs in the FM Mode, and every 13μs in the MFM Mode, or the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Read Data command.

If the processor terminates a read or write operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 4 shows the values for C, H, R, and N when the processor terminates the command.

Table 4. C, H, R, and N Values When Processor Terminates Commands

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: NC (No Change): The same value as the one at the beginning of command execution.
LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC in the Write Data mode. After the Write Data command is issued, the FDC loads the head, waits the specified head setting time, and begins reading ID fields. When all four bytes (C, H, R, and N) loaded during the command match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in the R register is incremented by one, and new data is written into the next data field. The FDC continues this Multisector Write Operation until a Terminal Count signal is issued. If a Terminal Count signal is sent to the FDC, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets Status register 1's DE flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

The Write command operates in the same manner as the Read command for the following items:

- Transfer capacity
- End of cylinder (EN) flag
- No data (ND) flag
- Head unload time interval
- ID information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

Refer to the Read Data command for details.

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer, then the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark, instead of the normal Data Address mark, is written at the beginning of the data field.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field and SK = 0, the FDC reads all the data in the sector and sets Status register 2's CM flag to 1, and terminates the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after

sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and, if there is no comparison, sets Status register 1's ND flag to 1. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hole for the second time, it sets Status register 1's Missing Address mark (MA) flag to 1 and terminates the command. (Status Register 0, bit 7 = 0, bit 6 = 1.)

Read ID

The Read ID command gives the present position of the recording head. The FDC stores the values from the first ID field it can read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, Status register 1's MA flag is set to 1; if no data is found, Status register 1's No Data (ND) flag is set to 1. The command is then terminated with STO bit 7 = 0 and bit 6 = 1. During this command, data transfer between FDC and the CPU occurs only during the result phase.

Format Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM 3740 Single Density format or IBM System 34 Double Density format, are recorded. The processor, during the command phase, supplies values i.e., Number of bytes/sector (N), Sectors Cylinder (SC), Gap Length (GPL), and Data Pattern (D) which determine the particular format to be written.

The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for Cylinder number (C), Head number (H), Sector number (R), and Number of bytes/sector (N). This allows diskette formatting with nonsequential sector numbers.

The processor must send new values for C, H, R, and N to the Z765A for each sector on the track. If FDC is set for the DMA mode, it issues four DMA requests per sector. If it is set for the Interrupt mode, it issues four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If the Fault signal is received from the FDD at the end of a Write operation, the FDC sets Status register 0's EC flag to 1 and terminates the command after setting Status register 0, bit 7 to 0 and bit 6 to 1. Also the loss of a Ready signal at the beginning of a command execution phase causes Status register 0, bit 7 and 6 to be set to 0 and 1 respectively.

Table 5 shows the sector size relationship between N, SC, and GPL.

Table 5. Functional Description of Commands

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
	8" Standard Floppy				
FM Mode	128 bytes sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
	5¼" Minifloppy				
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF

NOTES:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write format operation with 128 bytes sector (N = 00)

Scan Commands

The Scan commands allow comparison of data read from the diskette and data supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R) and the scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count (TC) signal is received.

If the conditions for scan are met, the FDC sets the Status register 2's Scan Hit (SH) flag to 1 and terminates the Scan command. If the conditions for scan are not met between the starting sector number (R) and the last sector on the cylinder (EOT), then the FDC sets Status register 2's Scan Not Satisfied (SN) flag to 1, and terminates the Scan command. During the scan operation, the receipt of a signal from the processor or DMA controller causes the FDC to complete the comparison of the particular byte in process and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of Scan.

Table 6.

	Status Register 2		
Command	**Bit 2 = SN**	**Bit 3 = SH**	**Comments**
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a Deleted Data Address mark on one of the sectors and SK = 0, then it regards the sector as the last sector on the cylinder, sets Status register 2's Control Mark (CM) flag to 1 and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark, reads the next sector, and sets Status register 2's Control Mark (CM) flag to 1 to show that a Deleted sector has been encountered.

When either the Step (STP) (contiguous sectors = 01 or alternate sectors = 02) sectors are read or the Multitrack (MT) is programmed, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following happens. Sectors 21, 23, and 25 are read, then the next sector, 26, is skipped and the index hole is encountered before the EOT value of 26 can be read resulting in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having Status register 1's Overrun (OR) flag set, it is necessary to have the data available in less than 27μs (FM mode) or 13μs (MFM mode). If an Overrun occurs, the FDC ends the command with Status register 0, bit 7 cleared to 0 and bit 6 set to 1.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. The FDC has four independent Present Cylinder registers for each drive which are cleared only after the Recalibrate command. The FDC compares the Present Cylinder Number (PCN) which is the current head position with the New Cylinder Number (NCN), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to 1, and Step Pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD cleared to 0, and Step Pulses are issued. (Step Out)

The rate at which Step pulses are issued is controlled by Stepping Rate Time (SRT) in the Specify command. After each Step pulse is issued NCN is compared against PCN, and when NCN = PCN, Status register 0's Seek End (SE) flag is set to 1, and the command is terminated. At this point FDC interrupt goes High. Bits D_0-D_3 in the Main Status register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state, but during the execution phase it is in the Nonbusy state. While the FDC is in the Nonbusy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a Not Ready state at the beginning of the command execution phase or during the Seek operation, then Status register 0's Not Ready (NR) flag is set to 1, and the command is terminated after bit 7 is set to 1 and bit 6 to 0.

If writing three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be 1ms shorter than that set in the Specify command.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is Low, the Direction signal remains 0 and step pulses are issued. When the Track 0 signal goes High, the Status register 0's SE flag is set to 1 and the command is terminated. If the Track 0 signal is still Low after 77 step pulses have been issued, the FDC sets Status register 0's SE and Equipment Check (EC) flags to 1s and terminates the command after Status register 0, bit 7 is cleared to 0 and bit 6 is set to 1.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command. If the Diskette has more than 77 tracks, the Recalibrate command should be issued twice, in order to position the Read/Write head to Track 0.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of command:
   - ☐ Read Data
   - ☐ Write Data
   - ☐ Write Deleted Data
   - ☐ Read Deleted Data
   - ☐ Read Track
   - ☐ Read ID
   - ☐ Format Track
   - ☐ Scan
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, D_5 in the Main Status Register is High. Upon entering the Result phase this bit is cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status command which resets the Interrupt signal and, via bits 5, 6, and 7 of Status register 0, identifies the cause of the interrupt (Table 7).

Table 7. Interrupt Identification

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk has reached the desired head position, the Z765A sets the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. Figure 6 is a graphic example.

Specify

The Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32ms...OF_{16} = 240ms). The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F = 1ms, E = 2ms, and D = 3ms). The Head Load Time (HLT) defines the time between the Head Load signal's going High and the start of the Read/Write operation. This timer is programmable from 2 to 254ms in increments of 2ms (01 = 2ms, 02 = 4ms, 03 = 6ms...7F = 254ms).

The time intervals mentioned are a direct function of the 8MHz clock; if the clock were reduced to 4MHz (minifloppy application), all time intervals would be increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the Non-DMA (ND) bit. When this bit is High (ND = 1), the Non-DMA mode is selected; when ND = 0, the DMA mode is selected.

Sense Drive Status

The processor uses this command to obtain the status of the FDDs. Status register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command (not defined above) is sent to the FDC, then the FDC terminates the command after Status Register 0 bit 7 is set to 1 and bit 6 to 0. No interrupt is generated by the Z765A during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status register are both High, indicating to the processor that the Z765A is in the Result phase and the contents of Status register 0 (STO) must be read. When the processor reads Status register 0, it finds an 80_H indicating the receipt of an Invalid command.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC considers the next command as an Invalid command.

This command may be used as a No-Op command to place the FDC in a standby or No Operation state.

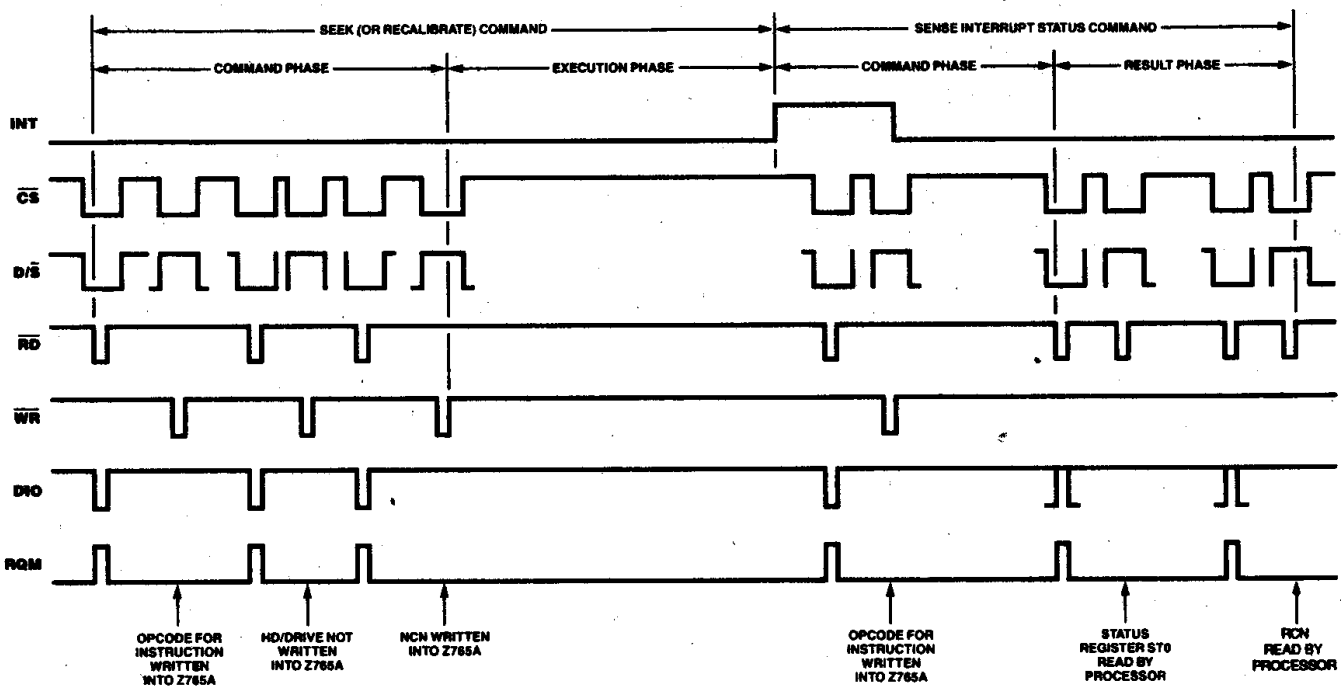


Figure 6. Seek, Recalibrate, and Sense Interrupt Status

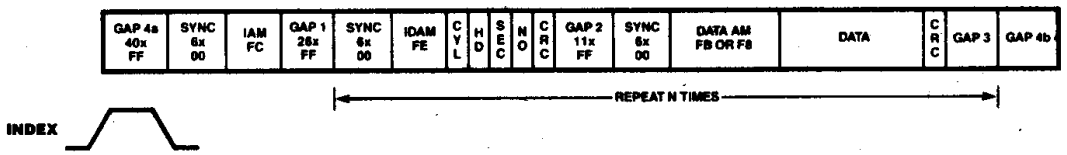


Figure 7. Data Format, FM Mode

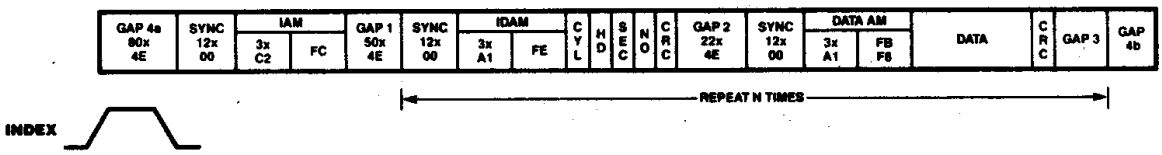


Figure 8. Data Format, MFM Mode

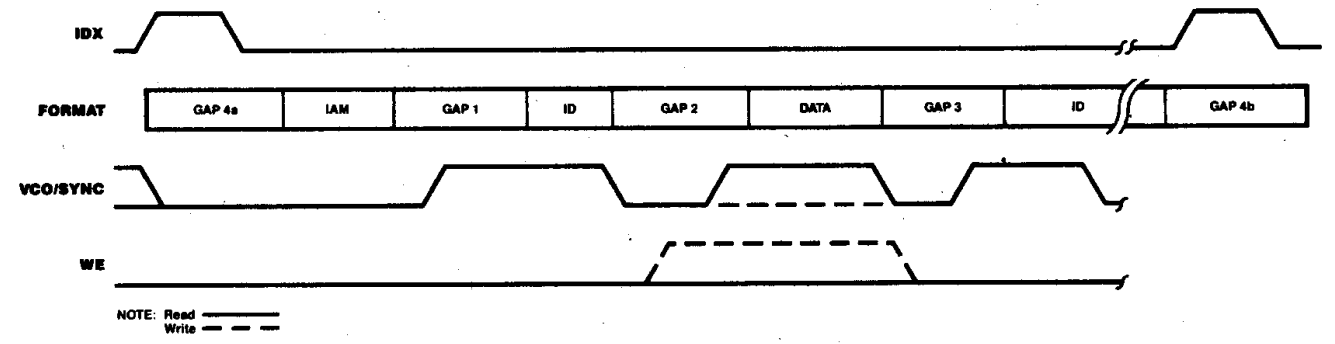


Figure 9. Data Timing Relationships

AC CHARACTERISTICS

T_A = −10°C to + 70°C; V_{CC} = +5V ± 5% unless otherwise specified.

Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
			120	125	500	ns	
1	TcC	Clock Cycle Time		125		ns	8" FDD
				250		ns	5¼" FDD
2	TwCh	Clock Width (High)	40			ns	
2a	TwCl	Clock Width (Low)	40			ns	
3	TrC	Clock Rise Time			20	ns	
4	TfC	Clock Fall Time			20	ns	
5	TsAR	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ to $\overline{RD}$ ↓ Setup Time	0			ns	
6	ThRA	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ from $\overline{RD}$ ↑ Hold Time	0			ns	
7	TwRD	$\overline{RD}$ Width	250			ns	
8	TdRDf (Do)	$\overline{RD}$ ↓ to Data Output Delay			200	ns	C_L = 100 pf
9	TdRDr (Dz)	$\overline{RD}$ ↑ to Data Float Delay	20		100	ns	C_L = 100 pf
10	TsCS(WRf)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) to $\overline{WR}$ ↓ Setup Time	0			ns	
11	ThCS(WRr)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) from $\overline{WR}$ ↑ Hold Time	0			ns	
12	TwWR	$\overline{WR}$ Width	250			ns	
13	TsD(WRr)	Data to $\overline{WR}$ ↑ Setup Time	150			ns	
14	ThD(WRr)	Data from $\overline{WR}$ ↑ Hold Time	5			ns	
15	TdRDr(INT)	$\overline{RD}$ ↑ to INT Delay Time			500	ns	
16	TdWRr(INT)	$\overline{WR}$ ↑ to INT Delay Time			500	ns	
17	TcDRQ	DRQ Cycle Time	13			µs	
18	TdDRQ(DACK)	$\overline{DACK}$ ↓ to DRQ ↓ Delay			200	ns	
19	TdDACK(DRQ)	DRQ ↑ to $\overline{DACK}$ ↓ Delay	200			ns	TcC = 125 ns
20	TwDACK	$\overline{DACK}$ Width	2			TcC	
21	TwTC	TC Width	1			TcC	
22	TwRST	Reset Width	14			TcC	
				4		µs	MFM = 0 5¼"
				2		µs	MFM = 1 5¼"
23	TcWCK	WCK Cycle Time		2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
24	TwWCKh	WCK Width (High)	80	250	350	ns	
25	TrWCK	WCK Rise Time			20	ns	
26	TfWCK	WCK Fall Time			20	ns	
27	TdWCKr(PS)	WCK ↑ to Preshift Delay Time	20		100	ns	
28	TdWCKr(WEr)	WCK ↑ to WE ↑ Delay Time	20		100	ns	
29	TdWCKr(WDA)	WCK ↑ to WDA Delay Time	20		100	ns	
30	TwRDDh	RDD Width (High)	40			ns	
				4		µs	MFM = 0 5¼"
				2		µs	MFM = 1 5¼"
31	TWCY	Window Cycle Time		2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
32	TsW(RDDh) ThW(RDDl)	Window to RDD ↑ Setup Time Window from RDD ↓ Hold Time	15			ns	
33	TsUS(RWh)	Unit Select to $\overline{RW}$/SEEK ↑ Setup Time	12			µs	
34	TsRWr(DIR)	$\overline{RW}$/SEEK ↑ to LCT/DIR Setup Time	7			µs	
35	TsDIR(STEPr)	LCT/DIR to STEP ↑ Setup Time	1			µs	
36	ThUS(STEPl)	Unit Select from STEP ↓ Hold Time	5			µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

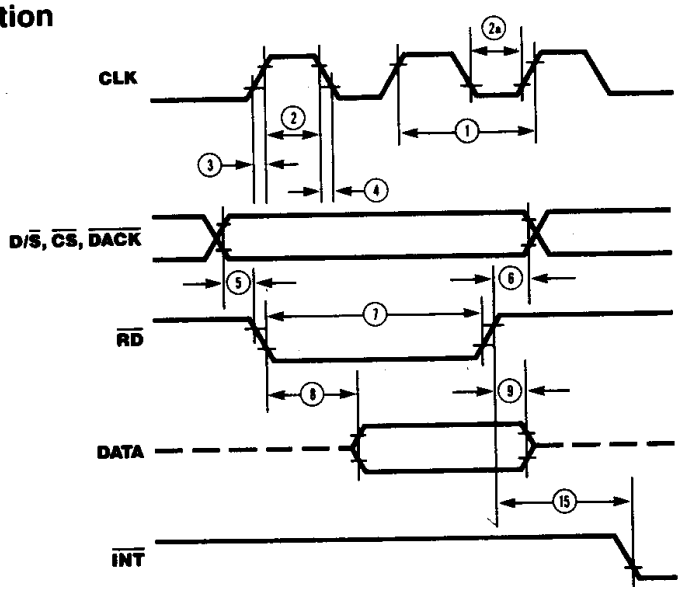
AC CHARACTERISTICS (Continued)

T_A = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

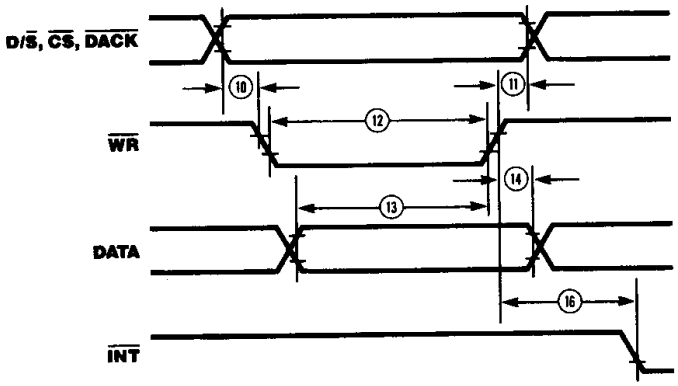
Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
37	TwSTEPh	STEP Width (High)	6	7	8	µs	
38	TcSTEP	STEP Cycle Time	16	Note 2	Note 2	µs	
39	TwFRh	FAULT RESET Width (High)	8		10	µs	
40	TwWDAh	Write Data (WDA) Width (High)	T_0-50			ns	
41	ThUS(SEEKf)	Unit Select from $\overline{RW}$/SEEK ↓ Hold Time	15			µs	
42	ThSEEK(DIR)	$\overline{RW}$/SEEK from LCT/DIR Hold Time	30			µs	
43	ThDIR(STEPf)	LCT/DIR from STEP ↓ Hold Time	24			µs	
44	TwIDX	INDEX Width (High and Low)	4			TcC	
45	TdDRQh(RDl)	DRQ ↑ to $\overline{RD}$ ↓ Delay Time	800			ns	
46	TdDRQh(WRl)	DRQ ↑ to $\overline{WR}$ ↓ Delay Time	250			ns	
47	TdDRQh(RWh)	DRQ ↑ to $\overline{RD}$ ↑ or $\overline{WR}$ ↑ Delay Time			12	µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

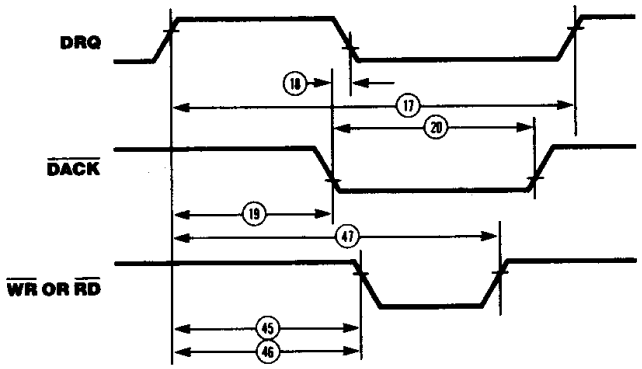
Processor Read Operation



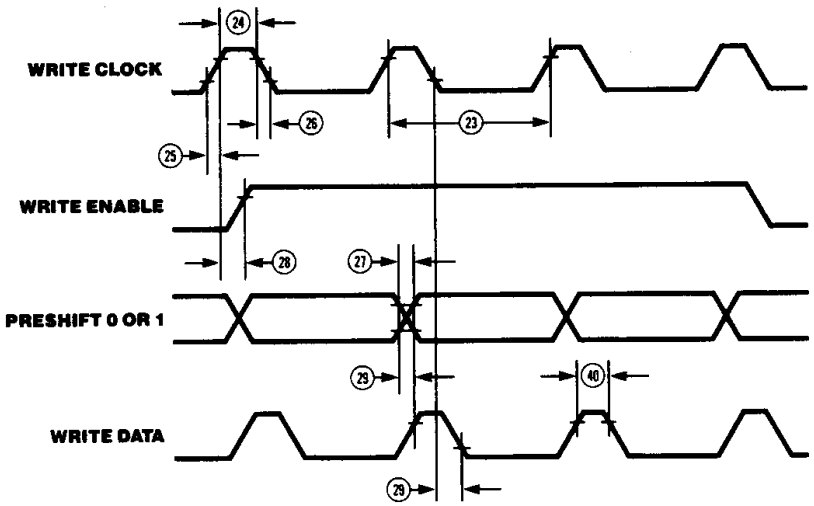
Processor Write Operation



DMA Operation

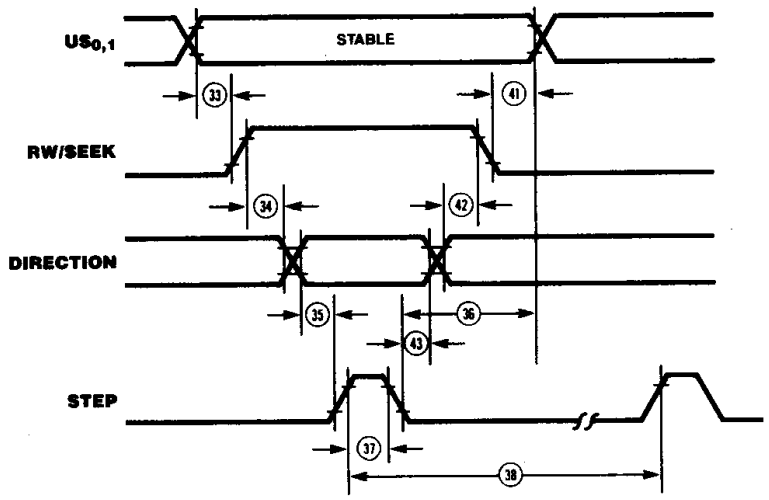


FDD Write Operation



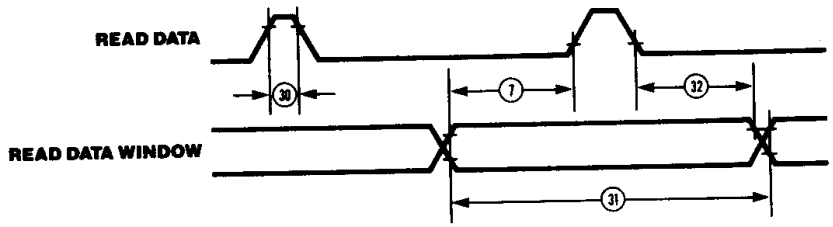
	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0

Seek Operation

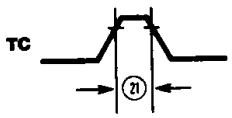


INDEX

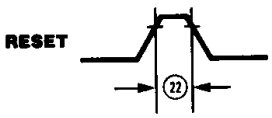
FDD Read Operation



Terminal Count



RESET



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating Temperature . . . . . 0°C to + 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output Voltages . . . . . −.5V to +7V
All Input Voltages . . . . . −.5V to +7V
Supply Voltage V_{CC} . . . . . −.5V to +7V
Power Dissipation 1W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Typ*	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −200 μA
V_{ILC}	Input Low Voltage (CLK + WR Clock)	−0.5		0.65	V	
V_{IHC}	Input High Voltage (CLK + WR Clock)	2.4		V_{CC} + 0.5	V	
I_{CC}	V_{CC} Supply Current			150	mA	
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = V_{CC}
				−10	μA	V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current			10	μA	V_{OUT} = V_{CC}
I_{LOL}	Low Level Output Leakage Current			−10	μA	V_{OUT} = +0.40V

*Typical values for T_A = 25°C and nominal supply voltage.

CAPACITANCE

T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{CLOCK}	Clock Input Capacitance		20	pF	All pins except pin under
C_{IN}	Input Capacitance		10	pF	test tied to AC Ground
C_{OUT}	Output Capacitance		20	pF	